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EXPERIMENTS IN TEXTURE PERCEPTION .

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Summary

Over the past year, a special graphics display has been constructed to further research in texture perception. This display has the ability to produce 440 x 440 point patterns consisting of complex (computer-generated) sinusoidal modulations of luminance that may be altered every 20 msec. A section of this report describes the 9 subsystems of the display, and elaborates its other capabilities, such as on-line variation of 100 x 100 random-dot (Julesz) patterns. With this display we are now in the process of determining the minimum number of spatial frequencies necessary to "match" one and two dimensional textures. Because such textures can be described exactly in terms of their Fourier components, the task is to determine just how many of these components are necessary to lead an observer to believe that the partially reconstructed texture is, in fact, the complete physical representation. At present, for linear one and two-dimensional texture patterns, only four spatial frequencies are sufficient to produce "texture metamers", at least for normal TV viewing conditions. Work is currently in progress to determine the generality of this finding, particularly for texture patterns composed of sinusoidal products.

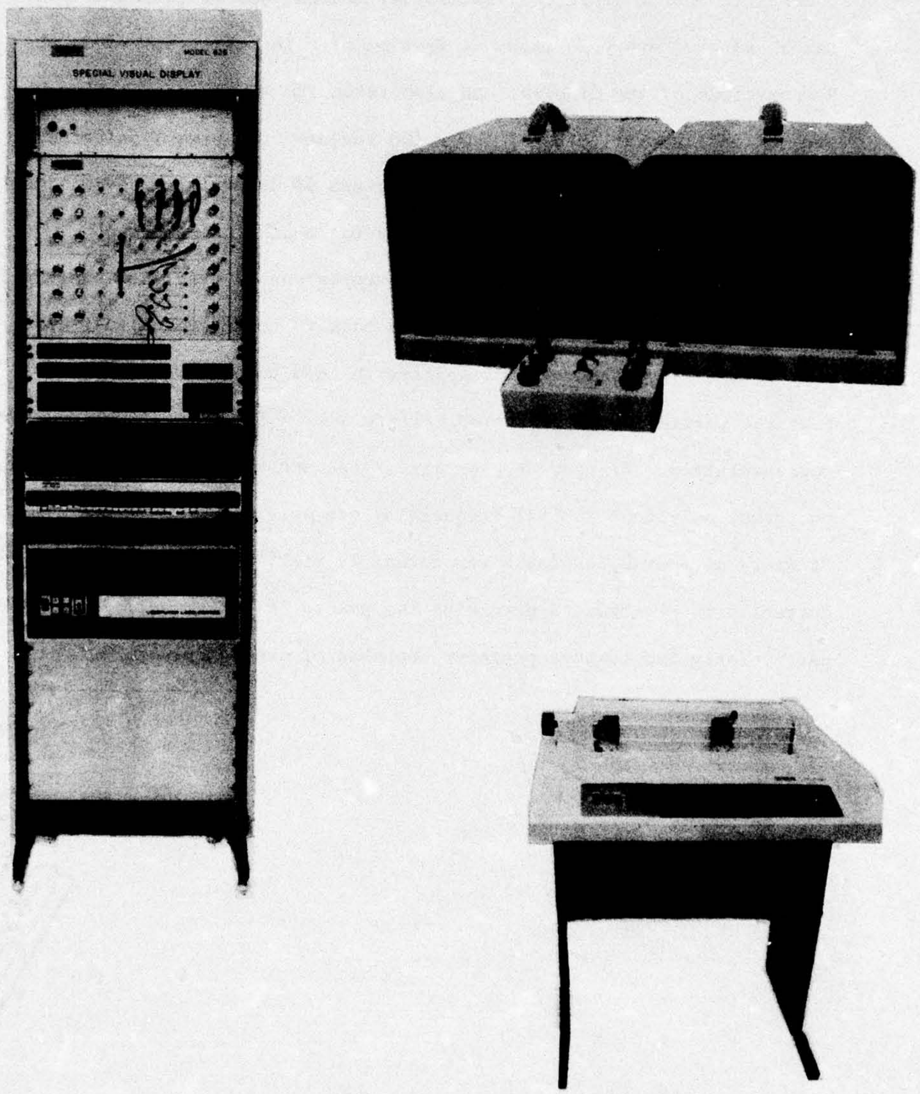

Figure 1

The special effects graphics display used to drive two TV monitors with 440 x 440 x 64 resolution. The device has 64K of 18 bit refresh memory, reprogramable for use as PDP 11 core. The disk capacity is 2.5 million words.

Contents

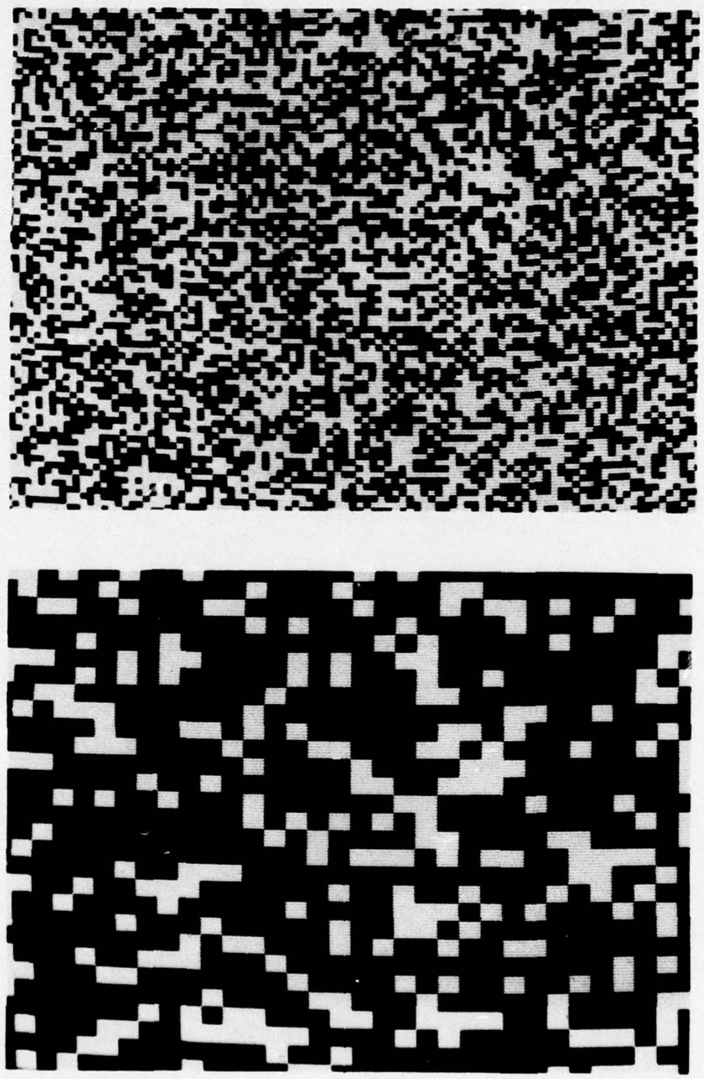

Figure 2

Two examples of simple random dot (Julesz) patterns generated by the display. Dot level luminance can range from 0 to 63. Patterns can be changed within 60 msec.

Experiments in Texture Perception

I. Introduction

Texture, like color, is one of the primary properties of an object (Metzger, 1926; Koffka, 1935). Yet only few studies of the texture recognition process have been made before 1960. Since this time, two technological advances have been made that have permitted visual scientists to begin to explore texture perception more fully. The first is the application of Fourier methods to visual perception. (Robson, 1966; Blakemore and Campbell, 1969) and the second is the availability of high-speed computers. The principal advantage gained by applying Fourier methods to vision has been the creation of a dimension - one of spatial frequency - into which the visual scientist can map the components of all patterns. Without this dimension, the study of texture perception has been handicapped in much the same way color vision studies would be impaired if the dimension of wavelength were not available. The second advance from computer technology allows one to now create easily many complex texture patterns having well-defined statistical or Fourier properties. The special graphics display takes advantage of both of these advances.

The novelty of our approach to human texture perception is that we are concerned only with describing textures that appear equivalent to one another. In the past, others have concentrated on the specification of the physical characteristics that will differentiate between all textures (See Bibliography). In contrast, our attempts to describe equivalent

textures are quite analogous to the development of color science where the primary concern is to identify spectral compositions that appear equivalent to the human observer. Such energy distributions that are physically different but appear equivalent are called metamers. Our approach to texture perception is to describe such metamers.

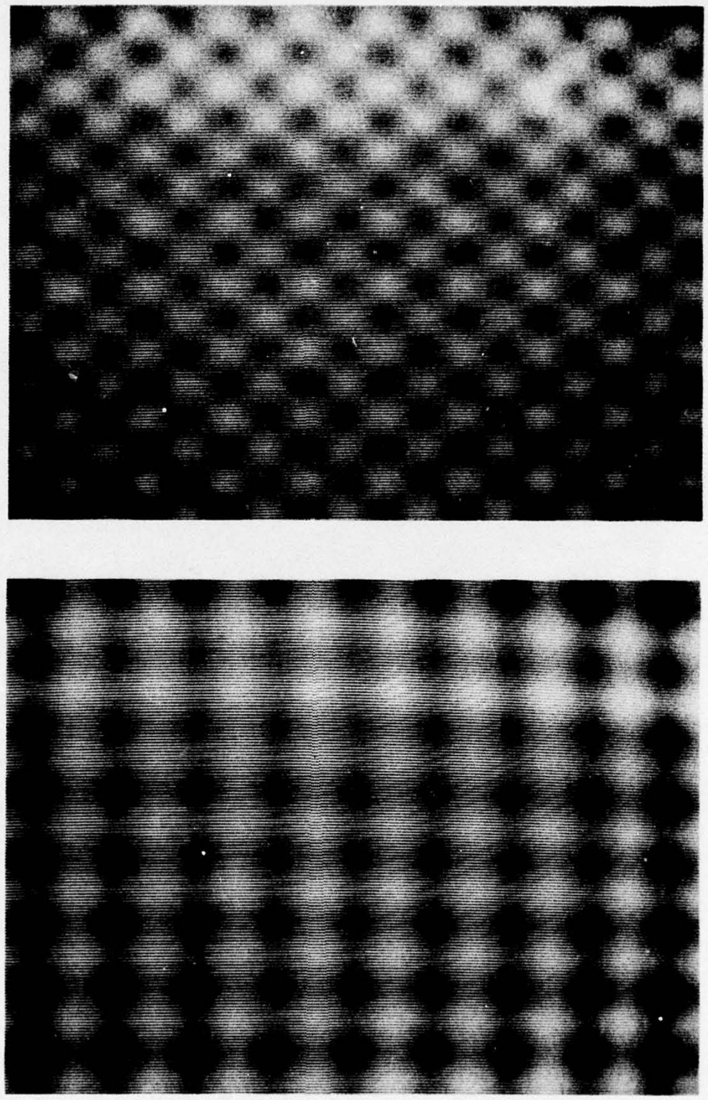

Figure 3

Example of the sums of a sinusoid (bottom) and the product of the same sinusoids (top). (Polaroid shots). Modulation amplitudes can be varied on-line.

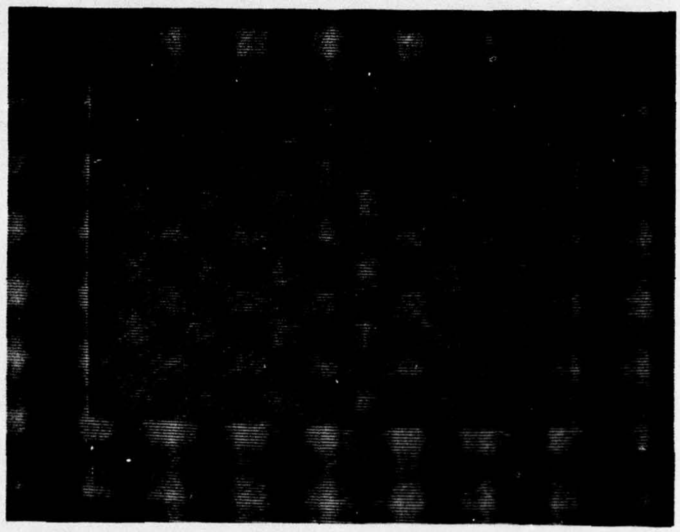

Figure 4

Pattern created using function generators and special effects modules. Inside rectangle contains the product of three sinusoids, the outside are the sums of the same sinusoids. (Polaroid shots). Modulation amplitudes of the components can be varied on-line.

II. Equipment

Special Graphics System

In order to generate texture patterns from their spatial frequency (Fourier) components, we have designed and have built a special graphics display. This display allows us to generate a 440 x 440 x 6 bit brightness pattern consisting of complex (computer-generated) sinusoids whose contrast may be altered every 20 msec. Both the sums and products of up to six components may be displayed with variable contrast. (Figure 3 shows examples of sums and products of one spatial frequency; Figure 4 shows a complex pattern.).

More specifically, the special visual display consists of 9 subsystems as follows:

1. Monitors: Conrac SNA 17/C (2)
   Monochrome television monitors
2. Operator Controls: Two channels, each with independent control of three sinusoidal or other component amplitudes and the a(x)*a(y) product term. Control boxes are on extension cables for convenience and flexibility of location. A six-channel A/D converter digitizes the control settings for input to the computer.
3. Function Table Computer: A dedicated PDP 11/10 Minicomputer is used to monitor the operator controls and calculate a(u) and b(u) function tables in accordance with the operator control settings,

where:

$$a(u) = \sum_{i=1}^{3} A_1 \sin(2\pi f_i u + \phi_i)$$

$$b(u) = \sum_{i=1}^{3} B_i \sin(2\pi f_i u + \phi_i)$$

4. <u>Video Function Generators</u>: Two identical custom designed video generators are provided to store the computed function tables and generate a video luminance signal of the form:

   $L_A(X,Y) = 1 + a(x) + a(y) + K_A a(x)\ a(y)$

   $L_B(X,Y) = 1 + b(x) + b(y) + K_B b(x)\ b(y)$

   Provision is made for adding an external video signal.

5. <u>Scan Generator</u>: A custom designed digital scan generator generates raster coordinates, synchronizing signals and control signals.

6. <u>Video Refresh System</u>: A custom-designed video refresh system is provided to allow an arbitrary two-dimensional pattern to be added to the texture display. The refresh system employs a standard core memory of 32,768 thirty-six bit words and can store 196,608 picture elements (pixels) with 6 bit (64 level) gray scale.

6. Video Refresh System (contd.):

The EMM Micromemory 3000 series has been used for the core memory. Four 3000DD (16K x 18 bit) cards are mounted in a 5 1/4" high chassis together with a control and video output card, power supply and cooling fans.

The control card circuit provides an alternate mode of operation in which four 108 x 108 checkerboard patterns can be stored and refreshed. The PDP-11/10 has control of mode selection and can select which of the four patterns is to be displayed.

If in the future, the video refresh capability should be no longer needed, the core memory can be easily converted on site to a general purpose RAM. EMM offers a Unibus interface for the Micromemory 3000 series. (See part (ii) of this section).

7. Video Interconnect Panel: A video interconnect panel is available to permit easy and flexible interconnection of video signals. The panel also contains eight adjustable DC voltage sources and a video integrator for use with the special effects generator and video multiplexer. The prints describing these components in more detail are given in Appendix I.

Memory Reconfiguration Interface

(with E. Black and A. Vezza)

An important component of the visual display is the refresh memory, which allows us to store and display any arbitrary pattern (or picture). However, this memory is not always in use, and rather that sitting idle, it is desirable to make it available to the PDP 11 to expand core. For example, the PDP 11 has an address space of only 32K of 16 bit words. The "memory reconfiguration interface" is a scheme for making the large amount of 18 bit word refresh memory available to the 16 bit work processor when the refresh capability is not needed. This interface thus allows the refresh memory to be used in modes other than for video storage, greatly increasing its versatility and usefulness at little increase in cost.

Example Illustrating Interface

A common processor is the PDP 11 which has an address space of 32K (K=1024) of 16 bit words. Because the I/O device interfaces take up 4K of the memory, the available program memory is 28K. Customarily, however, the processor is purchased with considerable less memory, for example only 12K (the minimum unit is 4K). Thus there is usually a considerable gap -- up to 24K -- between the top of the memory supplied with the processor and the I/O device interfaces. Depending on the configuration of the interface, this gap may be filled by the refresh memory.

In the above example where the processor came with 12K, the remaining 16K gap may be filled as follows:

Address	Size, Description
Bottom of Memory	
0	
	12K processor memory (furnished)
12K	
	16K refresh memory (optional)
28K	
	4K I/O device interfaces (furnished)
Top of Memory	

In the above example, 16K of refresh memory completely fills the unused portion of processor memory. In the event that only 12K of additional processor memory were needed, this 12K gap could be only partially filled with the reconfigured refresh memory based on 8K pages. A different reconfiguration, such as one based on 4K pages of memory would be required to completely fill a 12K memory gap.

For refresh memory reconfigured with 8K pages for processor use, there will be eight such pages to give the total of 64K of video memory necessary to refresh a 440*440 element display having 6 bit brightness levels. When this same memory is used by the processor, an 8K page must be selected by programming some control bits in an I/O buffer. Once this specification is accomplished, the processor must view the memory in terms of its normal 16 bit word, rather than as the 18 bit words used for video refresh. Again, this change is controlled by the processor, which allows either 8 or 9 bit bytes to be read or written from a 16 bit processor word. In refresh mode, four 9 bit processor transactions are reconfigured to give six 6 bit video bytes (total 36 bits in each case, or two 18 bit words), whereas in processor mode the same 36 bit unit is used to create two 16 bit words with four bits remaining. These 4

remaining bits may still be used, but there is a software cost in accessing them.

In the 9 bit mode, four page-select bits are required to select one out of sixteen 8K pages. In extra processor memory mode, however, only three page-select bits are required since there are half as many 18 bit words as 9 bit words. These reconfigurations are all accomplished by the interface so that regardless of the mode of use, the alterations in the memory are invisible to the user (i.e., the processor or refresh device).

Implementation

A) Specific case: PDP11/10 with 16K memory & Video refresh 64K by 18 bit words, 6 bit video.

The implementation at the reconfiguration interface is a fairly straightforward multiplexing of the address and data lines that control the core memory. For multiplexing data lines, the general scheme is to transfer half a processor word (8 bits) to and from half a memory word (9 bits). Thus two bits in the memory are ignored (these are the most significant bits of each half-word). When the processor needs to store or retrieve the full 9 bits of a memory half-word, it reconfigures the the interface so that the 9 least-significant processor bits are transferred to and from a memory half-word. In this case the upper (most-significant) 7 bits in the processor word are ignored.

The Scheme may be illustrated by the following table:

DATA MULTIPLEXING.

Reading (to CPU):

CPU bit	Processor mode	9-bit mode
p0 from	m0 or	m0, 9
p1	m1	m1, 10
p2	m2	m2, 11
p3	m3	m3, 12
p4	m4	m4, 13
p5	m5	m5, 14
p6	m6	m6, 15
p7	m7	m7, 16
p8	m9	m8, 17
p9	m10	-
p10	m11	-
p11	m12	-
p12	m13	-
p13	m14	-
p14	m15	-
p15	m16	-

Writing (from CPU):

Memory bit	Processor mode	9-bit mode
m0 from	p0	p0
m1	p1	p1
m2	p2	p2
m3	p3	p3
m4	p4	p4
m5	p5	p5
m6	p6	p6
m7	p7	p7
m8	-	p8
m9	p8	p0
m10	p9	p1
m11	p10	p2
m12	p11	p3
m13	p12	p4
m14	p13	p5
m15	p14	p6
m16	p15	p7
m17	-	p8

Note: pi indicates a processor bit number, mi a memory bit number.

The figure is best viewed as two tables, one for reading, and one for writing. In each case the target device bit numbers are in the left-most column (CPU for reading, Memory for writing). Let us first consider the processor mode. Here we are concerned with the first two columns in each table. When writing, we see that processor bit 0 (p0) is written into memory bit 0, similarly, p1 is written into memory bit one, and so on up to p7. Nothing is stored in memory bit 8, since the processor has one bit less than the memory in each half-word. The second memory half-word has bits numbered 9-17, for a total of 9 again. The processor has bits numbered p8-p15, and once again, the lowest bit from the processor byte is paired

with the lowest bit of the memory byte. Thus we see p8 is written into memory bit 9, etc., and nothing is written into bit 17.

In order to retrieve what was written, the read operation in this mode must simply reverse the bit mappings, and this is seen in the first two columns of the read table. Here the processor is the target (first column): memory bit 0 (m0) will be read into processor bit 0, and so on up to m7 and processor bit 7. Now the next most significant processor bit is bit 8, which was written into memory bit 9 because of the byte-length difference. Thus we see that on reading, m9 must be read into processor bit 8. The most significant processor bit is bit 15, which is seen to be read back from memory bit 16 (m16), and once again, m17 is ignored.

In the 9 bit mode, things are a little more tricky, as may be seen in the rightmost column of each table. Consider writing: here, the processor is sending a 9 bit byte in its bits numbered p0-p8. These bits are written into either the high or low byte of memory (depending on an address bit). Therefore bits p0-p8 appear opposite both bytes, memory bits 0-8 and 9-17. When reading, the inverse map must be performed so that CPU bits 0-8 retrieve the high or low byte (depending on the same address bit). Thus both m0-m8 and m9-m17 appear as candidates to get read into the nine processor bits -- the particular byte is selected by a multiplexor that is switched by the byte addressing bit in the reconfiguration interface.

ADDRESS MULTIPLEXING.

Address multiplexing is necessary because of the conflicts which arise in addressing the EMM memory both normally and in a 9-bit byte mode. Because of the conflicts, the addresses which are generated by the CPU during an instruction must be interpreted differently by the memory, depending on the mode of addressing being used. The normal mode is described first:

The PDP 11 has a 32K address space. It takes sixteen bits to address such a space. The EMM memory was designed to fill one quarter of that space and so has fourteen bits of address available (two bits are required to specify one of four quarters). Since the EMM memory requires seventeen bits to specify a byte uniquely, there remains a need to generate three more bits. These three remaining bits are written into an I/O buffer, and select one-eighth of the EMM memory (two raised to the third power is eight) until such time as the program changes them.

In 9 bit byte mode, the CPU can not use its built-in byte operations, since one cannot assume that more than eight bits (a PDP 11 byte) will be presented to the memory. A word transaction (16 bits) must be used to specify a byte of memory, effectively reducing the number of address lines by one. An extra bit in the I/O register must therefore be used for this mode.

The address mappings are chosen to provide uniform access across modes -- sequential bytes are retrieved in either processor or 9 bit byte mode in the order in which they would be displayed in refresh graphics mode.

The following table illustrates the address multiplexing:

Address bits:

Memory address	Processor mode	9 bit mode	
ma 0	pa 0	pa 1	; byte selection
ma 1	pa 1	pa 2	; first word address bit
ma 2	pa 2	pa 3	; second word address bit
ma 3	pa 3	pa 4	
ma 4	pa 4	pa 5	
ma 5	pa 5	pa 6	
ma 6	pa 6	pa 7	
ma 7	pa 7	pa 8	
ma 8	pa 8	pa 9	
ma 9	pa 9	pa10	
ma10	pa10	pa11	
ma11	pa11	pa12	
ma12	pa12	pa13	
ma13	pa13	i/o bit 0	; 4K page selection
ma14	i/o bit 0	i/o bit 1	; 8K page selection
ma15	i/o bit 1	i/o bit 2	; 16K page selection
ma16	i/o bit 2	i/o bit 3	; 32K page selection

Note: pa i indicates a CPU address (on the unibus)
ma i indicates a memory address bit.

B) General case:

Although implementation of the reconfiguration interface is described and implemented in terms of a specific case, the scheme has generality to a wide variety of other applications. Whenever excess memory based upon words of bit length M is available, the same scheme can be used to reconfigure the memory for use by another system utilizing words of length (M-n) bits.

III. Experiments

Although most of the past year has been devoted to the fabrication of equipment and the creation of software packages, some preliminary experiments have begun using the graphics display.

i.) One Dimensional Textures are vertical (or horizontal) sinusoidal patterns. (See previous annual report for examples). Rather than begin as before and duplicate our measurements of "texture matching functions" (Richards and Polit, 1974), we have tried to determine in a different manner the number of spatial frequency primaries necessary to match all patterns with components ranging from 1/4 to 30 c/deg. This new method assumes a fixed form for a texture primary, as characterized by the inset to figure 5. Along a log spatial frequency axis, the primary function has one positive lobe flanked by two negative lobes. (Both lobes have been found to be necessary to create texture metamers). We can now ask the experimental question of how large a separation may be present between the location of adjacent primaries for texture equivalence to hold. The answer is obtained by measuring the acceptability of texture matches between frequency f (a variable) and the primaries which bear a fixed relation to f. The relation is as follows:

$$\begin{aligned} 0.5\ (f) + A\ (k^{3/2}f) + B\ (K^{-3/2}f) \\ \equiv \quad C\ (k^{1/2}f) + D\ (k^{-1/2}f) \end{aligned} \qquad (1)$$

where the contrast of f is held fixed at 0.5 and A - D are the measured contrasts of the primary frequencies ($k^x f$).

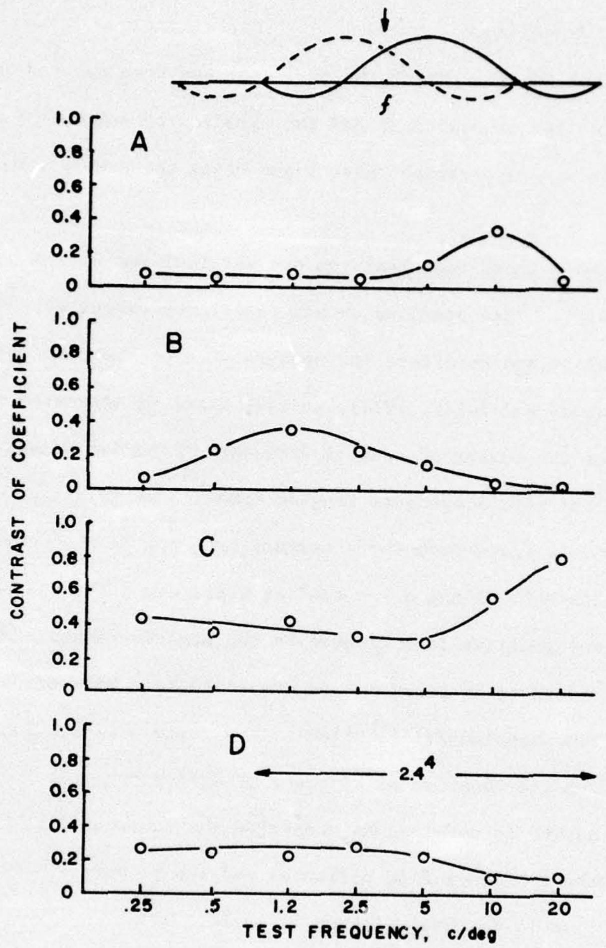

Figure 5

Test to determine the minimum bandwidth necessary for texture primaries. The waveform of the primaries is shown in the inset. See text equation (1) for the description of the relations between the primaries. Each graph shows the contrast of a primary eneded to match the spatial frequency given on the abscissa.

Figure 5 shows the values of the coefficients A - D for values of f ranging from 1/4 to 20 c/deg. These values do not change much as k is altered from 2 to 3, but the acceptability of the texture matches does. Excellent texture equivalences can be obtained only if k is less than 2.4. Thus, the "half-width" of a primary is of this magnitude, and four primaries can span a range of only $2.4^4 = 31$. For practical purposes, however, this range is quite acceptable, covering all patterns except those with luminance "gradents" less than 25% per degree.

Note that all coefficients have constant values over a wide portion of the range examined. This important porperty permits a further simplification, for if the coefficient values were flat everywhere, then texture matches would be invariant over visual angle or fixation distance. At the lower spatial frequencies, a partial size constancy is obtained. At higher spatial frequencies, the failure in constancy is due to failures in the resolution of the highest spatial frequency components.

ii.) Two Dimensional Patterns are created either by summing vertical and horizontal sinusoids, or by taking their product, or both. For the sums of sinusoids, the behavior at threshold and suprathreshold is similar to the one dimensional patterns. This implies independent processing of the vertical and horizontal components of our patterns, an observation quite in accord with single unit electrophysiology (Hubel and Wiesel, 1962). The visibility and behavior of two dimensional products, on the other hand, can not be so easily predicted. (See Figures 3 and 4 for patterns of each type).

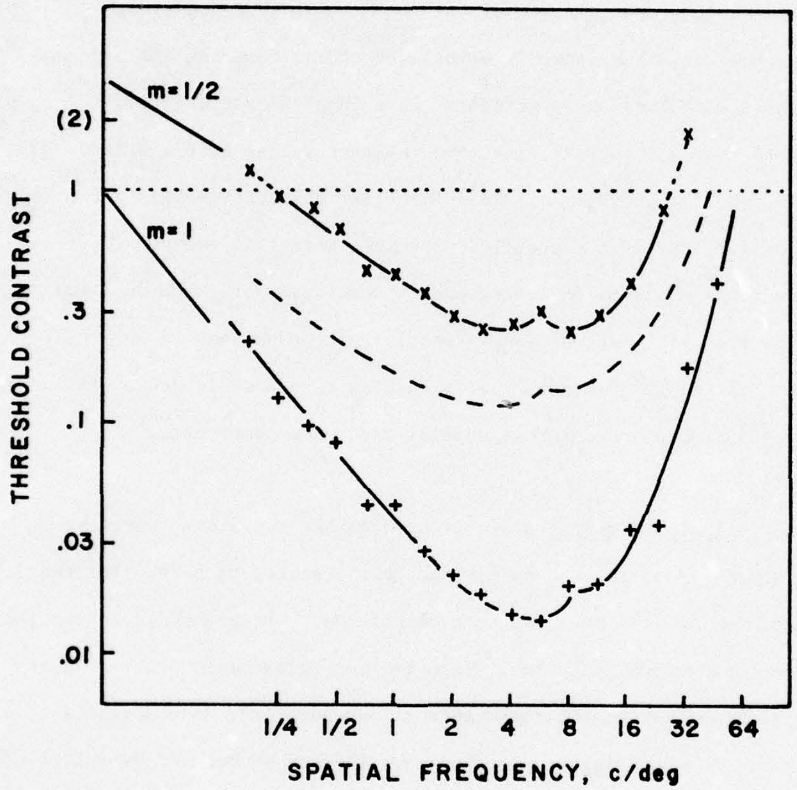

Figure 6

Threshold contrast for the sums of a pure sinusoid (plusses) and for the products (crosses). The threshold for the products is higher than predicted by a simple peak to trough model for detectability.

Fig. 6 shows threshold contrast at several spatial frequencies for both the sums and products of pure sinusoidal patterns. The lowest envelope (plusses) is the sensitivity curve for patterns made up of the sum (vertical and horizontal) of a single spatial frequency. Given these data, it should be possible to predict the threshold for the products (crosses). Because the modulation amplitude for the product is reduced by taking the square of the modulation, threshold contrast for products should be the square-root of the threshold for the sums. This is the dashed curve. Instead, the product threshold is 2x higher. This difference is approximately what would be expected if linear summation along a sinusoid occured for the sums (i.e., analysis by a "simple" or "complex" feature detector) but where such summation did not occur for the products (i.e. analysis by a simple concentric field - a "Kuffler" unit).

From these preliminary threshold measurements, therefore, we expect that textures built from the sums of sinusoids will have properties quite different from those built from the products.

iii.) Random-dot Textures can easily be created on our system, with variable statistics, gradients, or displacements. We have now completed (with S. Purks) a study of the discrimination of random-dot textures with variable nth gram statistics. Contrary to an early proposal by Julesz (1962) we have found many classes of patterns differing in their 3rd or higher nth-gram statistics that are easily discriminable. An example of one such pattern is given in Fig. 7.

Figure 7

Two different strings differing only in their 4th order are juxtaposed. The difference between the left and right halves is visible, contrary to earlier proposals about strings differing only in higher order statistics.

IV. Projections

Texture is one of the primary properties of an object. Like color, texture is a quality which helps the human observer to define and identify objects. Yet we know very little about human texture perception. What is its basis? How good are we at identifying textures? Are we as good as a Fourier pattern analyser? At present, the most important aspect of the research suggests that texture analysis is performed by only four "filters". Thus, all (one-dimensional) textures may be completely specified in terms of only four primaries, at least over the range of focal vision. Such a specification will describe all equivalences between textures. This is a nontrivial accomplishment. In the domain of color perception, if it were necessary to describe all colors in terms of its precise wavelength composition, then the transmission of chromatic information would not have become a feasible possibility. The fact that the human observer filters the wavelength spectrum allows us to build economical communication systems for chromatic information. By the same token, if it may be demonstrated that the human observer analyses textures on the basis of only a few filters, then a considerable saving in the transmission of texture information may be gained. This practical benefit far outweighs, but in no way diminishes the further gains that we will achieve in our understanding of the human visual system.

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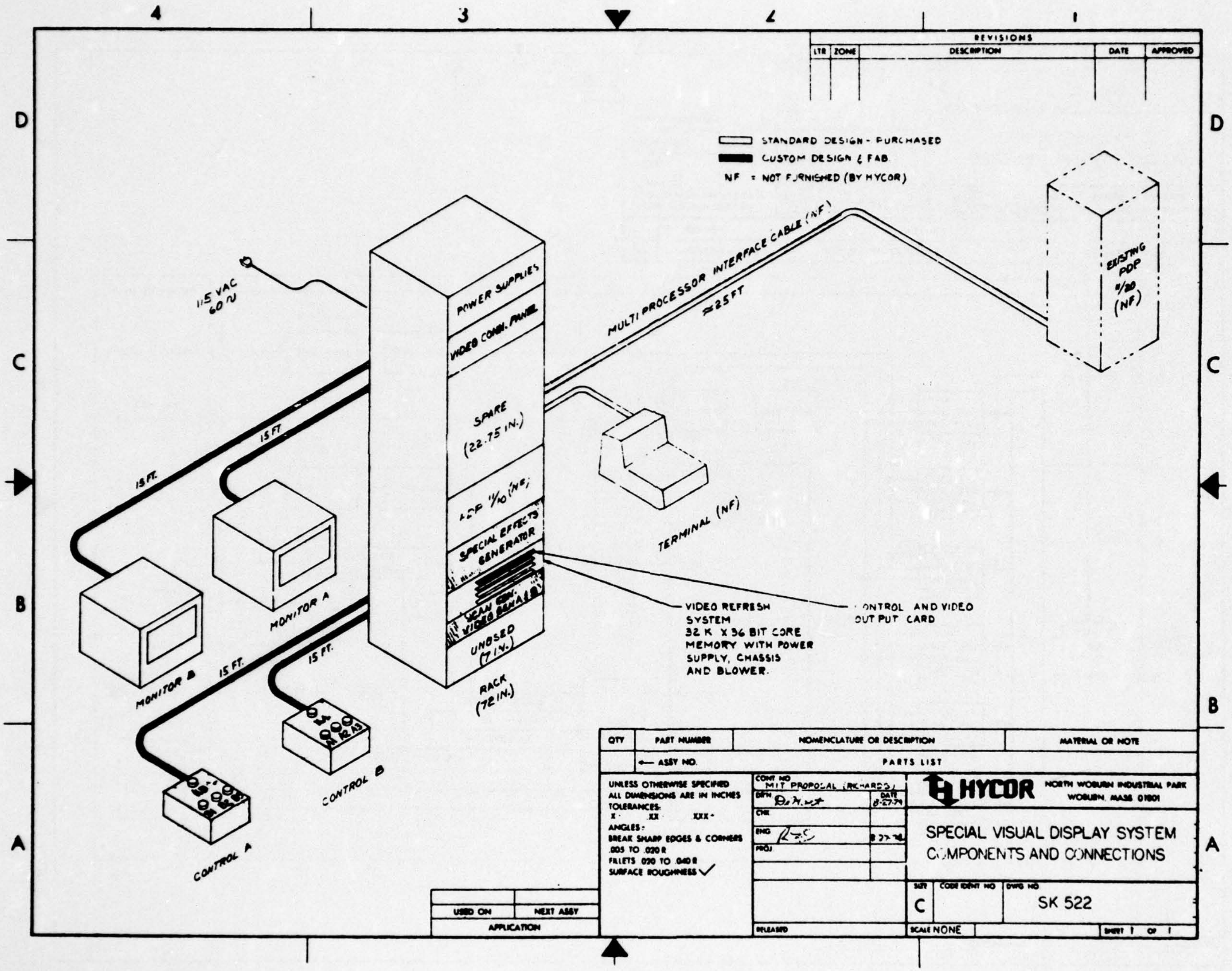
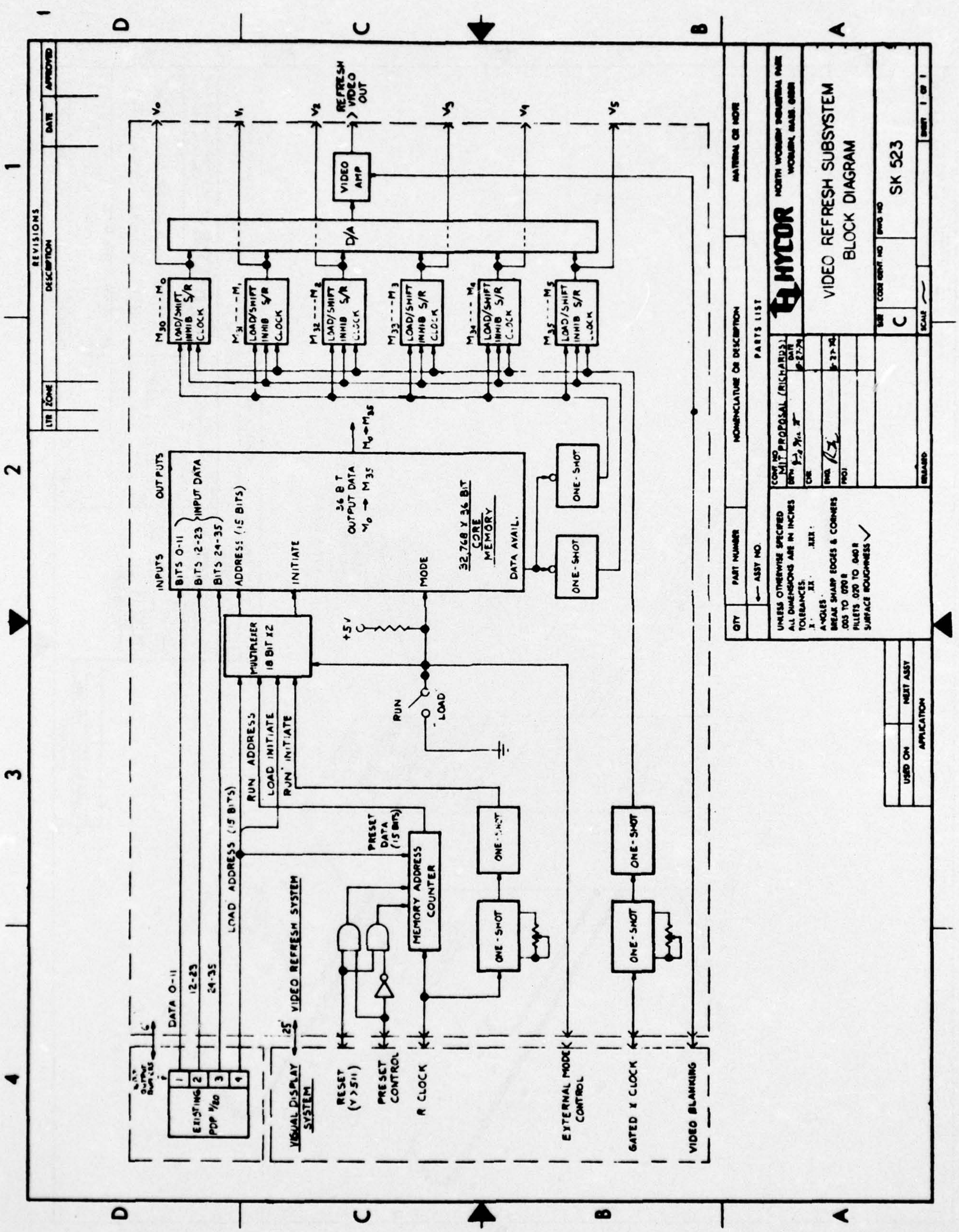
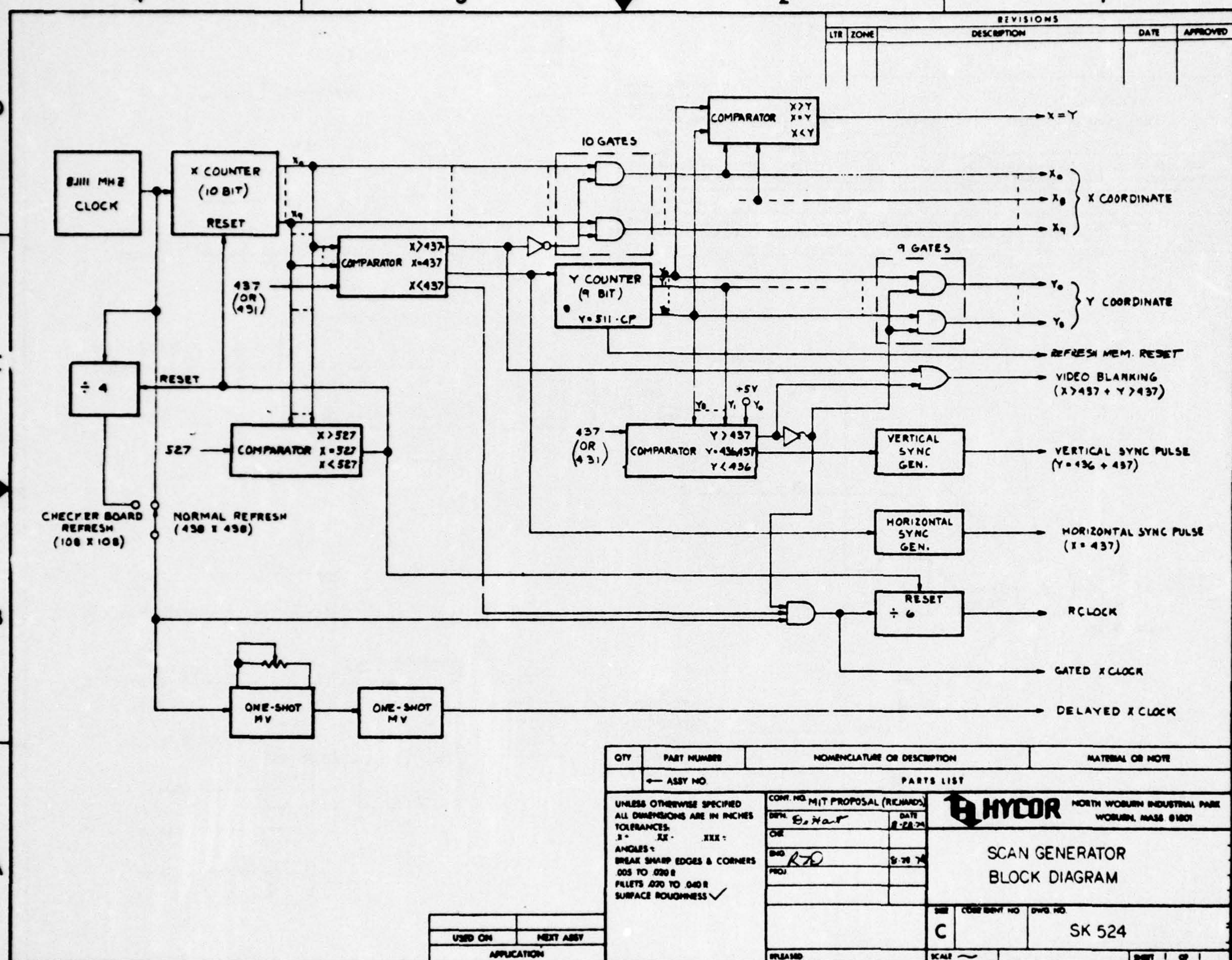
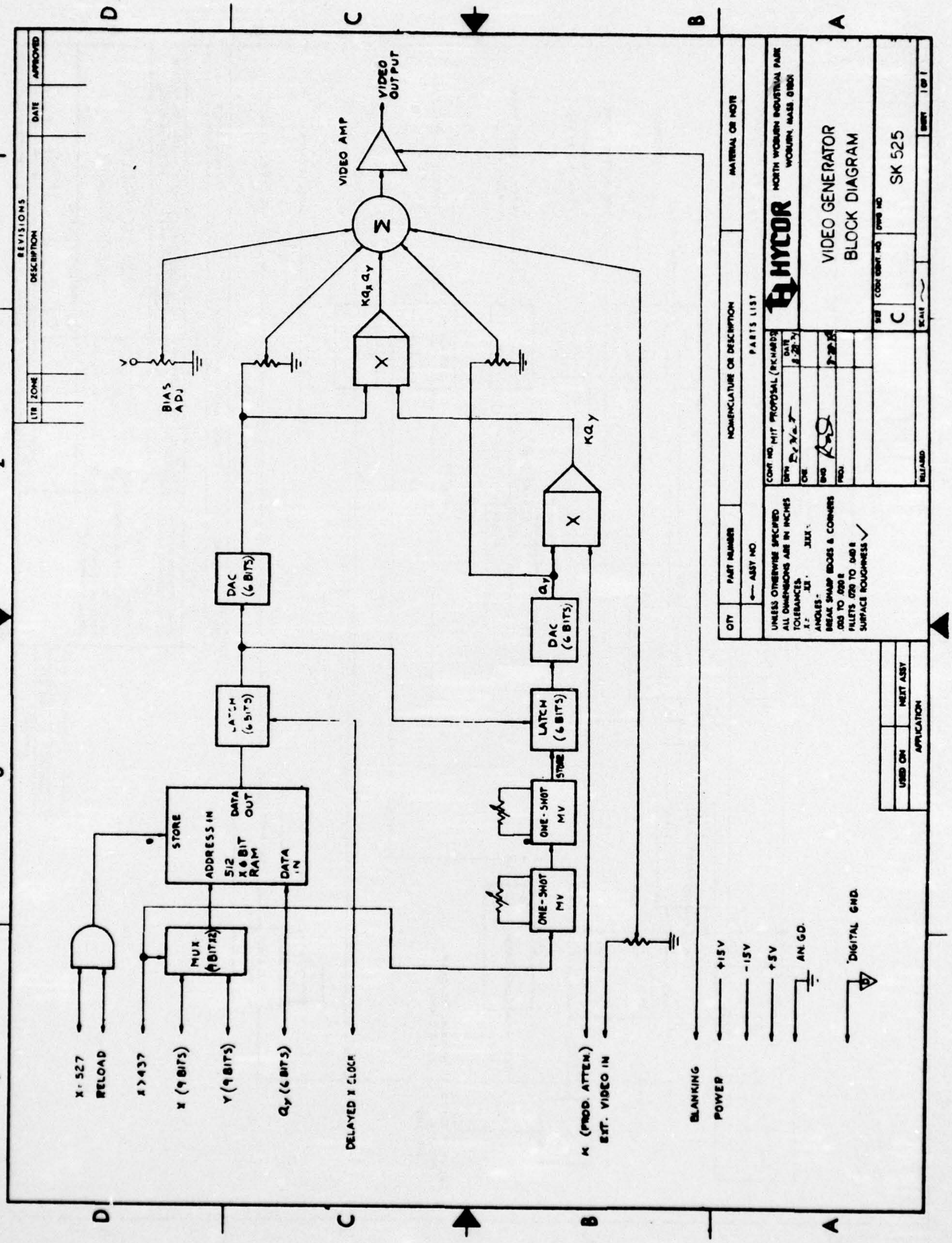
VIII. Appendix

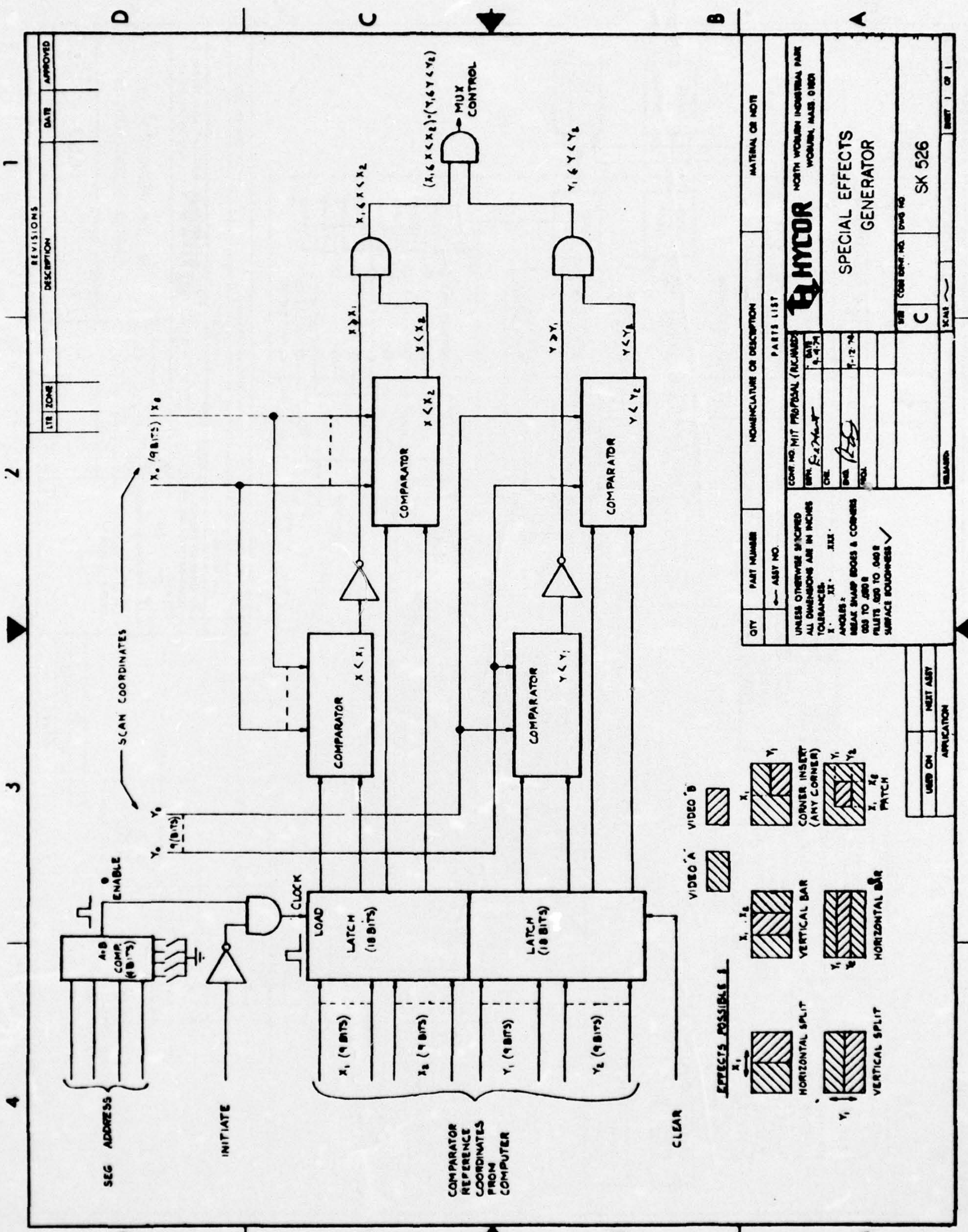


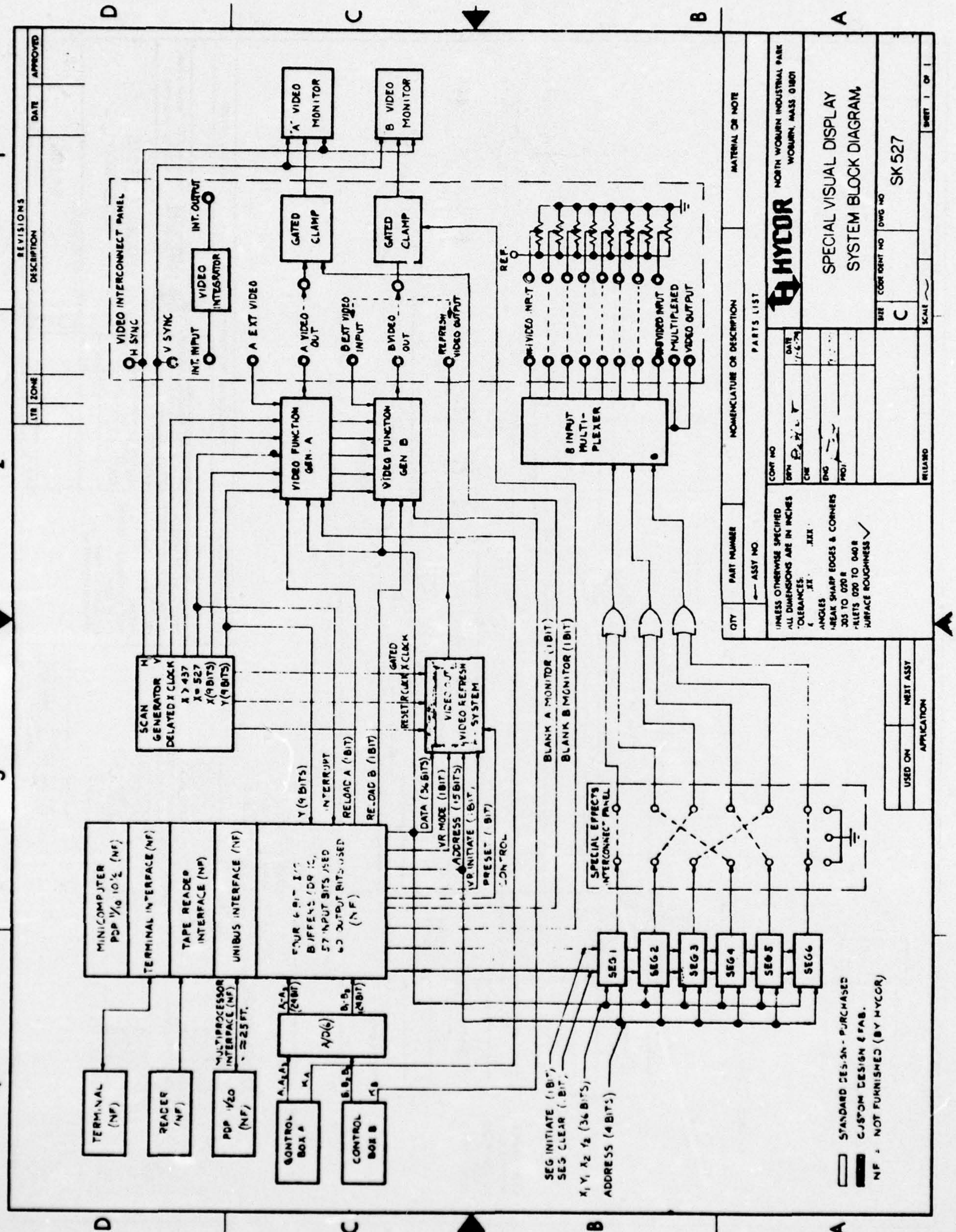
REVISIONS
LTR | ZONE | DESCRIPTION | DATE | APPROVED
STANDARD DESIGN - PURCHASED
CUSTOM DESIGN & FAB.
NF = NOT FURNISHED (BY HYCOR)
115 VAC 60 ~
POWER SUPPLIES
VIDEO CONN. PANEL
SPARE (22.75 IN.)
SPECIAL EFFECTS GENERATOR
UNUSED (7 IN.)
RACK (72 IN.)
MULTI PROCESSOR INTERFACE CABLE (NF) ≈25 FT
EXISTING PDP 11/20 (NF)
TERMINAL (NF)
15 FT.
MONITOR A
MONITOR B
CONTROL A
CONTROL B
VIDEO REFRESH SYSTEM 32 K X 36 BIT CORE MEMORY WITH POWER SUPPLY, CHASSIS AND BLOWER.
CONTROL AND VIDEO OUTPUT CARD
QTY | PART NUMBER | NOMENCLATURE OR DESCRIPTION | MATERIAL OR NOTE
ASSY NO. | PARTS LIST
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES
TOLERANCES: .X .XX .XXX
ANGLES:
BREAK SHARP EDGES & CORNERS .005 TO .020 R
FILLETS .020 TO .040 R
SURFACE ROUGHNESS ✓
CONT NO MIT PROPOSAL (RICHARDS)
DATE 8-27-74
HYCOR NORTH WOBURN INDUSTRIAL PARK WOBURN, MASS 01801
SPECIAL VISUAL DISPLAY SYSTEM COMPONENTS AND CONNECTIONS
SIZE C
CODE IDENT NO
DWG NO SK 522
SCALE NONE
SHEET 1 OF 1
USED ON | NEXT ASSY
APPLICATION
RELEASED


REVISIONS
LTR
ZONE
DESCRIPTION
DATE
APPROVED
EXISTING PDP 1/20
DATA 0-11
12-23
24-35
LOAD ADDRESS (15 BITS)
VIDEO REFRESH SYSTEM
VISUAL DISPLAY SYSTEM
RESET (Y>511)
PRESET CONTROL
R CLOCK
EXTERNAL MODE CONTROL
GATED X CLOCK
VIDEO BLANKING
MEMORY ADDRESS COUNTER
PRESET DATA (15 BITS)
ONE-SHOT
RUN ADDRESS
LOAD INITIATE
RUN INITIATE
MULTIPLEXER 18 BIT X2
+5V
RUN
LOAD
INPUTS
BITS 0-11
BITS 12-23
BITS 24-35
INPUT DATA
ADDRESS (15 BITS)
INITIATE
MODE
OUTPUTS
36 BIT OUTPUT DATA $M_0 \rightarrow M_{35}$
32,768 X 36 BIT CORE MEMORY
DATA AVAIL.
$M_0 \rightarrow M_{35}$
LOAD/SHIFT INHIB S/R CLOCK
$M_{30} --- M_0$
$M_{31} --- M_1$
$M_{32} --- M_2$
$M_{33} --- M_3$
$M_{34} --- M_4$
$M_{35} --- M_5$
D/A
VIDEO AMP
V_0
V_1
V_2
V_3
V_4
V_5
REFRESH VIDEO OUT
QTY
PART NUMBER
NOMENCLATURE OR DESCRIPTION
MATERIAL OR NOTE
PARTS LIST
ASSY NO.
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES
TOLERANCES:
ANGLES:
BREAK SHARP EDGES & CORNERS
FILLETS
SURFACE ROUGHNESS
CONT NO
MIT PROPOSAL (RICHARDS)
DRN
CHK
ENG
PROJ
RELEASED
HYCOR
NORTH WOBURN INDUSTRIAL PARK WOBURN, MASS.
VIDEO REFRESH SUBSYSTEM BLOCK DIAGRAM
SIZE
C
CODE IDENT NO
DWG NO
SK 523
SCALE
SHEET 1 OF 1
USED ON
NEXT ASSY
APPLICATION


8.111 MHZ CLOCK
X COUNTER (10 BIT) RESET
10 GATES
COMPARATOR X>Y X=Y X<Y
X=Y
X COORDINATE
COMPARATOR X>437 X=437 X<437
437 (OR 431)
Y COUNTER (9 BIT) Y=511·CP
9 GATES
Y COORDINATE
REFRESH MEM. RESET
VIDEO BLANKING (X>437 + Y>437)
+5V
437 (OR 431)
COMPARATOR Y>437 Y=436,437 Y<436
VERTICAL SYNC GEN.
VERTICAL SYNC PULSE (Y=436 + 437)
÷ 4
RESET
527
COMPARATOR X>527 X=527 X<527
CHECKER BOARD REFRESH (108 X 108)
NORMAL REFRESH (438 X 438)
HORIZONTAL SYNC GEN.
HORIZONTAL SYNC PULSE (X=437)
RESET ÷ 6
RCLOCK
GATED X CLOCK
ONE-SHOT MV
ONE-SHOT MV
DELAYED X CLOCK
REVISIONS
LTR ZONE DESCRIPTION DATE APPROVED
QTY PART NUMBER NOMENCLATURE OR DESCRIPTION MATERIAL OR NOTE
ASSY NO. PARTS LIST
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES
BREAK SHARP EDGES & CORNERS .005 TO .020 R
FILLETS .020 TO .040 R
SURFACE ROUGHNESS
CONT. NO. MIT PROPOSAL (RICHARDS)
HYCOR
NORTH WOBURN INDUSTRIAL PARK WOBURN, MASS 01801
SCAN GENERATOR BLOCK DIAGRAM
C
SK 524
USED ON NEXT ASSY
APPLICATION
RELEASED
SCALE
SHEET 1 OF 1


VIDEO GENERATOR
BLOCK DIAGRAM
SK 525
HYCOR
NORTH WOBURN INDUSTRIAL PARK
WOBURN, MASS. 01801
MIT PROPOSAL (RKH4052)
VIDEO AMP
VIDEO OUTPUT
BIAS ADJ
DAC (6 BITS)
LATCH (6 BITS)
STORE
ADDRESS IN
512 X 6 BIT RAM
DATA OUT
DATA IN
MUX (9 BITS)
ONE-SHOT MV
X = 527
RELOAD
X (9 BITS)
Y (9 BITS)
DELAYED X CLOCK
EXT. VIDEO IN
BLANKING
POWER
+15V
-15V
+5V
AN. GD.
DIGITAL GND.
REVISIONS
DESCRIPTION
DATE
APPROVED
PARTS LIST
APPLICATION
USED ON
NEXT ASSY


SEG ADDRESS
INITIATE
COMPARATOR REFERENCE COORDINATES FROM COMPUTER
CLEAR
ENABLE
CLOCK
LOAD
LATCH (18 BITS)
LATCH (18 BITS)
SCAN COORDINATES
COMPARATOR
COMPARATOR
COMPARATOR
COMPARATOR
MUX CONTROL
EFFECTS POSSIBLE
HORIZONTAL SPLIT
VERTICAL SPLIT
VERTICAL BAR
HORIZONTAL BAR
CORNER INSERT (ANY CORNER)
PATCH
VIDEO 'A'
VIDEO 'B'
REVISIONS
PARTS LIST
HYCOR
NORTH WOBURN INDUSTRIAL PARK WOBURN, MASS. 01801
SPECIAL EFFECTS GENERATOR
SK 526


REVISIONS
LTR
ZONE
DESCRIPTION
DATE
APPROVED
VIDEO INTERCONNECT PANEL
H SYNC
V SYNC
INT. INPUT
VIDEO INTEGRATOR
INT. OUTPUT
A EXT VIDEO
A VIDEO OUT
B EXT VIDEO INPUT
B VIDEO OUT
REFRESH VIDEO OUTPUT
GATED CLAMP
GATED CLAMP
'A' VIDEO MONITOR
B VIDEO MONITOR
REF.
VIDEO INPUT
VIDEO INPUT
MULTIPLEXED VIDEO OUTPUT
8 INPUT MULTI-PLEXER
VIDEO FUNCTION GEN. A
VIDEO FUNCTION GEN B
SCAN GENERATOR
DELAYED X CLOCK
X > 437
X = 527
X (9 BITS)
Y (9 BITS)
H
V
GATED X CLOCK
RESET
CLEAR
VIDEO OUT
VIDEO REFRESH SYSTEM
BLANK A MONITOR (1 BIT)
BLANK B MONITOR (1 BIT)
MINICOMPUTER PDP 11/10 10'2 (NF)
TERMINAL INTERFACE (NF)
TAPE READER INTERFACE (NF)
UNIBUS INTERFACE (NF)
FOUR 6-BIT I/O BUFFERS (DR 11C, 57 INPUT BITS USED 63 OUTPUT BITS USED) (NF)
Y (9 BITS)
INTERRUPT
RELOAD A (1 BIT)
RELOAD B (1 BIT)
DATA (36 BITS)
VR MODE (1 BIT)
ADDRESS (15 BITS)
VR INITIATE (1 BIT)
PRESET (1 BIT)
CONTROL
SPECIAL EFFECTS INTERCONNECT PANEL
SEG 1
SEG 2
SEG 3
SEG 4
SEG 5
SEG 6
A/D(6)
(24 BIT)
(24 BIT)
MULTIPROCESSOR INTERFACE (NF)
≈ 25 FT.
TERMINAL (NF)
READER (NF)
PDP 11/20 (NF)
CONTROL BOX A
CONTROL BOX B
SEG INITIATE (1 BIT)
SEG CLEAR (1 BIT)
$X_1 Y_1 X_2 Y_2$ (36 BITS)
ADDRESS (4 BITS)
STANDARD DESIGN - PURCHASED
CUSTOM DESIGN & FAB.
NF : NOT FURNISHED (BY HYCOR)
QTY
PART NUMBER
ASSY NO
NOMENCLATURE OR DESCRIPTION
MATERIAL OR NOTE
PARTS LIST
UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE IN INCHES
TOLERANCES
ANGLES
BREAK SHARP EDGES & CORNERS
FILLETS
SURFACE ROUGHNESS
CONT NO
DFTN
CHK
ENG
PROJ
RELEASED
DATE
HYCOR
NORTH WOBURN INDUSTRIAL PARK WOBURN, MASS 01801
SPECIAL VISUAL DISPLAY SYSTEM BLOCK DIAGRAM
SIZE C
CODE IDENT NO
DWG NO
SK 527
SCALE
SHEET 1 OF 1
USED ON
NEXT ASSY
APPLICATION

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE		READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER AFOSR - TR - 76 - 1312	2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle) EXPERIMENTS IN TEXTURE PERCEPTION		5. TYPE OF REPORT & PERIOD COVERED Scientific Interum Report 1 June 75 through 31 May 76
		6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s) Whitman A. Richards		8. CONTRACT OR GRANT NUMBER(s) F44620-74-C-0076
9. PERFORMING ORGANIZATION NAME AND ADDRESS Massachusetts Institute of Technology 77 Massachusetts Avenue Cambridge, Mass. 02139		10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS 61101E/2765/681313
11. CONTROLLING OFFICE NAME AND ADDRESS Advanced Research Projects Agency Building 410 Bolling Air Force Base, D. C. 20332		12. REPORT DATE July, 1976
		13. NUMBER OF PAGES 37
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office) Air Force Office of Scientific Research (NL) Building 410 Bolling Air Force Base, D. C. 20332		15. SECURITY CLASS. (of this report) Unclassified
		15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Vision, Texture Perception, Graphics Display

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Over the past year, a special graphics display has been constructed to further research in texture perception. This display has the ability to produce 440 x 440 point patterns consisting of complex (computer-generated) sinusoidal modulations of luminance that may be altered every 20 msec. A section of this report describes the 9 subsystems of the display, and elaborates its other capabilities, such as on-line variation of 100 x 100 random-dot (Julesz) patterns. With this display we are now in the process of determining

Over

cont

the minimum number of spatial frequencies necessary to "match" one and two dimensional textures. Because such textures can be described exactly in terms of their Fourier components, the task is to determine just how many of these components are necessary to lead an observer to believe that the partially reconstructed texture is, in fact, the complete physical representation. At present, for linear one and two-dimensional texture patterns, only four spatial frequencies are sufficient to produce "texture metamers", at least for normal TV viewing conditions. Work is currently in progress to determine the generality of this finding, particularly for texture patterns composed of sinusoidal products.

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

REPORT DOCUMENTATION PAGE

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4. TITLE (and Subtitle)

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5. TYPE OF REPORT & PERIOD COVERED

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Whitman A. Richards

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403 698

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Massachusetts Institute of Technology
77 Massachusetts Avenue
Cambridge, Mass. 02139

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Unclassified

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